Spiral Inductors and Transmission Lines in Silicon Technology Using Copper–Damascene Interconnects and Low-Loss Substrates

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***Abstract*—Spiral inductors and different types of transmission lines are fabricated by using copper (Cu)–damascene interconnects and high-resistivity silicon (HRS) or sapphire substrates. The fabrication process is compatible with the concepts of silicon device fabrication. Spiral inductors with 1.4-nH inductance have quality factors (Q) of 30 at 5.2 GHz and 40 at 5.8 GHz for the HRS and the sapphire substrates, respectively. 80-nH inductors have $Q's$ as high as 13. The transmission-line losses are near 4 dB/cm at 10 GHz for microstrips, inverted microstrips, and coplanar lines, which are sufficiently small for maximum line lengths within typical silicon-chip areas. This paper shows that inductors with high $Q's$ for lumped-element designs in the 1–10-GHz range and transmission lines with low losses for distributed-element designs beyond 10 GHz can be made available with the proposed adjustments to commercial silicon technology.**

***Index Terms*—Inductors, lumped-element microwave circuits, MMIC's, planar transmission lines, silicon materials/devices.**

I. Introduction

THE emerging mass production of wireless hand-held radio transceivers presents a challenge to any technology, since device performance, power consumption, volume manufacturability, and cost all play a significant role. Silicon technology is a prominent candidate to satisfy the high-volume and low-cost requirements for this market, but some investments in process development will have to be made to meet the performance requirements. The energy losses in the interconnect metal and the silicon substrate in particular, present serious limitations for high-frequency operation of integrated inductors and transmission lines, which are not as evident for other technology candidates such as GaAs monolithic microwave integrated circuits (MMIC's) or hybrids. The common aluminum (Al) metallization used in silicon technology is not as thick and has roughly twice the resistivity of gold (Au) interconnects used in GaAs MMIC's. The resistivity of conventional silicon substrates is about 10 Ωcm in comparison to the semi-insulating GaAs where it is essentially infinite.

The quality-factor (Q) of an inductor is particularly sensitive to these constraints. The spiral inductor has, therefore, a comparably lower Q than a capacitor on a silicon substrate [1] and is the performance-limiting device in lumped-element designs in the 1–10-GHz range. Much of the recent research related to radio-frequency (RF) systems on silicon has, therefore, been devoted to this passive component [1]–[12]. The general concept of an inductor integrated on a silicon substrate considers the formation of a spiral coil at one metal level and an underpass contact at a second metal level. The challenge of overcoming the mentioned limits has been addressed by exploiting multilevel interconnect technology (more than two metal layers) in two different ways: an effectively thick conductor has been formed by shunting several metal layers together [1], [5]–[7], and the lowest metal layers have been omitted in order to increase the spacing between spiral coil and substrate, which reduces the oxide capacitance and makes the effect of the substrate resistivity less significant [6], [7]. The highest demonstrated Q factors exceeded 20, which required five levels of interconnects [6], [7]. The advantage of this approach was the fact that it used a commercial fabrication process which was readily available. The use of multilevel interconnects also allowed an extension to a multilevel spiral structure [8], [9], which provided a lower dc resistance for a given inductance [9]. Other approaches have considered replacement of the Al by Au to improve the metal resistivity or used high-resistivity silicon (HRS), quartz, sapphire, or micromachining to lower the substrate losses at the price of deviating from conventional fabrication processes [10]–[13].

Beyond 10 GHz, the Q available with the lumped-element designs may not be sufficient and distributed elements may be needed. That will require transmission lines with low losses at high frequencies at which energy is dissipated at a considerable level through dielectric polarization. Also, for transmission lines as for inductors, both the ohmic losses in the conductor and substrate, and the dielectric losses in the interconnect isolation and substrate have to be minimized.

In this paper, we describe an approach for the integration of transmission lines and spiral inductors, in which copper (Cu) metallization was used either over HRS or over sapphire substrates. A conventional silicon substrate was used as control. In Section II, we show the fabrication process. The results for a large variety of inductor structures are given and discussed in Section III, including those of comparable Al devices. In Section IV, the characteristics of different types of transmission lines, which were fabricated by using the novel process, are shown and compared. A summary of the findings and some conclusions are given in Section V.

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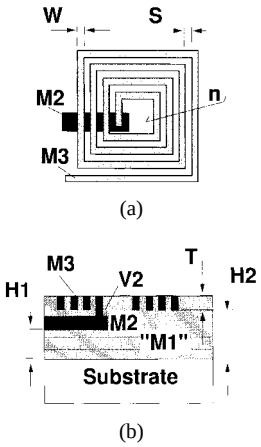


Fig. 1. Spiral inductor structure in (a) plan view and (b) cross section. The spiral coil was built using the $M3$ metal layer, and the underpass contact was at $M2$. The layer $M1$ was not used.

II. Fabrication Process and High-Frequency Characterization

A three-level Cu–damascene process with 2.5-μm-thick Cu interconnects and oxide (SiO_2) isolation, which was similar to the fabrication process described in [14], was developed to build spiral inductor structures and different types of transmission lines at the upper two metal levels ($M2$ and $M3$ in Figs. 1 and 2). The first metal level ($M1$) was not used in our experiments, but the corresponding dielectric thicknesses were incorporated, as illustrated in Figs. 1(b) and 2(a)–(c). This allowed a comparison to other experimental results based on a three-level Al process [15] and better meets the interconnect requirements for a fully monolithic RF transceiver circuit. In the experiments, we compared three different types of substrates, i.e., 10-Ωcm silicon (Cu1), float-zone silicon [Cu2, $>$1000 Ωcm (HRS)], and sapphire (Cu3). The metallization was similar for the three cases. Processing started with a deposition of a thick oxide film on the substrates. A first lithographic mask level was used to partially recess the oxide to define the underpass contact of the inductor ($M2$ in Figs. 1 and 2). A liner film, which acts as a diffusion barrier and adhesion promoter, was deposited first. A Cu film was deposited next to refill the etched groove, and chemical–mechanical polishing (CMP) was applied to remove the Cu overburden from the oxide-field region without any significant effect on the groove Cu refill. The exposed Cu surface was capped to improve the adhesion of the subsequent oxide film. As a result of the liner and the cap films, a direct contact of Cu to oxide was avoided. The combination of oxide etch, Cu refill, and planarization is known as the Cu–damascene process [14]. The thickness of layer $M2$ was 4 μm. After planarization, a second oxide film was deposited and a second mask level was used to locally recess the oxide surface for the formation of the spiral inductor coils and the transmission lines ($M3$ in Figs. 1 and 2). A third mask level was used to define locations for etching the oxide film down to the underlying Cu layer in order to form via contacts [$V2$ in Fig. 1(b)]. Both the $V2$ and the $M3$ openings were refilled by one Cu deposition, and a single planarization step was used to remove the Cu overburden (dual-damascene process). The thickness of $M3$ was 2.7 μm for Cu1 and Cu3, while it was only 2.4 μm for Cu2 due to rework. The Cu–damascene interconnects offer three advantages over conventional Al metallization. First, the Cu resistivity is only 1.9 $\mu\Omega$cm which is about half of the Al value (actually Al with a small percentage of Cu). Second, both metal layers and vias are formed in Cu, in comparison to Al technology where tungsten (W) vias are used, so that the contact and via resistances are smaller. Third, the damascene process provides thicker metal layers and wider and taller vias compared to the conventional interconnect schemes. This results in a smaller line resistance and a larger spacing of the spiral coil from the substrate. The Cu-interconnect process is capable of providing a metal pitch as required for VLSI circuits, even though the inductor structures fabricated here had coarse dimensions [12], [14].

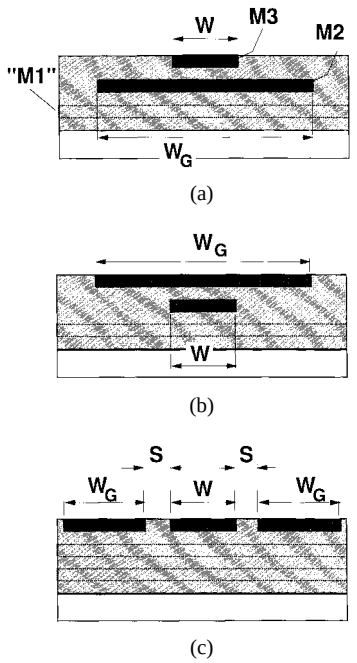


Fig. 2. Plan and cross-sectional views of (a) microstrip, (b) inverted microstrip, and (c) coplanar transmission lines. The dashed rectangles shows the location of unused metal lines in the three-metal level process. The width of the signal line (W), the width of the ground line (W_G), and the space between signal and ground (S) are indicated.

For comparisons, two Al-interconnect processes with three (Al1) or five (Al2) metal levels, which have been used in previous experiments [7], [15], are described in Table I, together with the Cu processes. The lateral dimensions of some of the inductors that were fabricated are listed in Table II. The inductor structures were the same as the ones used in [6] and [14].

One- and two-port S-parameter measurements were performed for the inductor (Fig. 3) and transmission-line characterizations, respectively. Measurements up to 20 GHz were carried out on-wafer using high-frequency coplanar probes and an HP-8720B network analyzer. Signal–ground (SG) probes were used for the inductors, and the transmission lines were measured by using ground–signal–ground (GSG) probes. Parasitics associated with the network-analyzer input stage, the coaxial cables and the high-frequency probes were de-embedded first by using open, short, and load structures on

TABLE I
PROCESS AND STRUCTURAL INFORMATION ON THE CU–DAMASCENE PROCESSES Cu1–Cu3 AND THE AL CONTROLS Al1 AND Al2

Process	Metal Layers in Coil	Metal Thickness (T) and Type	Substrate Resistivity and Type	Underpass/ Substrate Spacing (H1)	Coil/ Substrate Spacing (H2)
Al1	M3	2 μm AlCu	10 ohm-cm Si	3.6 μm	5.7 μm
Al2	M3/M4/M5	4 μm AlCu	10 ohm-cm Si	4.5 μm	7.0 μm
Cu1	M3	2.7 μm Cu	10 ohm-cm Si	4.5 μm	6.3 μm
Cu2	M3	2.4 μm Cu	HRS-Si	4.5 μm	6.6 μm
Cu3	M3	2.7 μm Cu	Sapphire	4.5 μm	6.3 μm

TABLE II
LATERAL DIMENSIONS OF THE INDUCTOR STRUCTURES

	LA2	LA4	LB2	LB5	LB8
Area	500x500μm	500x500μm	226x226μm	226x226μm	226x226μm
No. of Turns (n)	16	8	3	4	6
Wire-Width (W)	9 μm	22 μm	18 μm	16 μm	12 μm
Wire-Space (S)	4 μm	4 μm	18 μm	10 μm	4 μm

a CASCADE Microtech ISS calibration set. Then, the S_{11} of a dummy device, which consisted only of the inductor probe pads, was measured (SG probes only). After probing the inductor test devices (which included a set of probe pads and a spiral inductor structure each), the Y_{11} of the probe pads was subtracted from the inductor's Y_{11}. The correction associated with the dummy device was about 10%–20%. The error in de-embedding the contact resistance was not more than 0.2 Ω.

III. HIGH-Q SPIRAL INDUCTORS

From the S-parameters, the impedance of the inductors was derived as $Z = 50\ \Omega \times (1+S_{11})/(1-S_{11})$. The inductance of the device was calculated as $L = \mathrm{Im}(Z)/\omega$ and the unloaded Q factor as $Q = \mathrm{Im}(Z)/\mathrm{Re}(Z)$. The frequency-dependent values for L and Q of the inductors $LB2$ and $LA2$ (Table II) are shown in Figs. 4 and 5, respectively. For the discussion of the results, it is helpful to compare them to the lumped-element model in Fig. 6. There, the spiral coil of the inductor is modeled as an ideal inductance L_S in series with a resistance R_S, both in parallel with an inter-wire capacitance C_P. The substrate isolation is represented by two capacitances C_{Ox} and bulk resistances R_B. A substrate contact can, in principle, be considered between the two R_B resistors, but in our experiments the substrate was left floating since the contact would be marginal or not effective for the HRS and sapphire substrates.

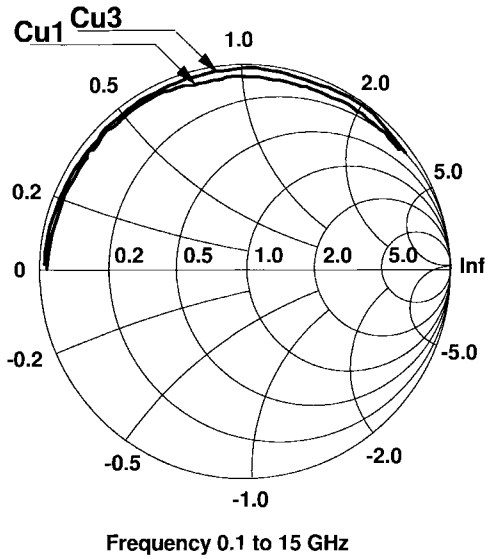


Fig. 3. Smith chart with measured S_{11} parameters of $LB2$ structures fabricated by using the processes Cu1 (10-Ωcm Si), and Cu3 (Sapphire).

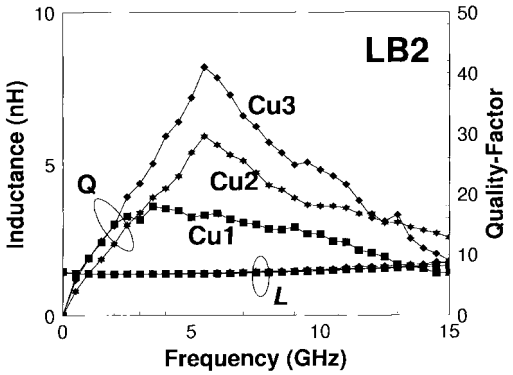


Fig. 4. Inductance and quality-factor as functions of frequency for $LB2$ structures fabricated by using processes Cu1 (10-Ωcm Si), Cu2 (HRS), and Cu3 (Sapphire).

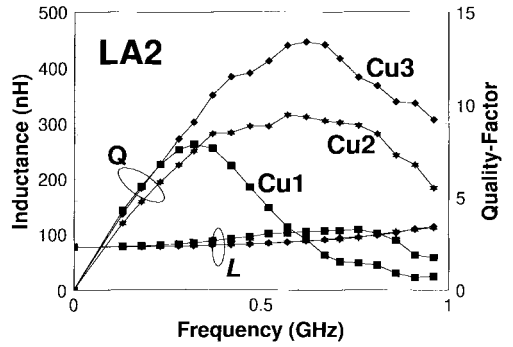


Fig. 5. Inductance and Q factor as functions of frequency for $LA2$ structures fabricated by using processes Cu1 (10-W-cm Si), Cu2 (HRS), and Cu3 (Sapphire).

A comparison of the measured inductance and Q's *versus* frequency of the inductor $LB2$, which was fabricated by using the process Cu1 (10-Ωcm Si), to the simulated characteristics, using the model in Fig. 6, is shown in Fig. 7. An overall good agreement was observed in spite of the simplicity of the inductor model. The model-element parameters are listed

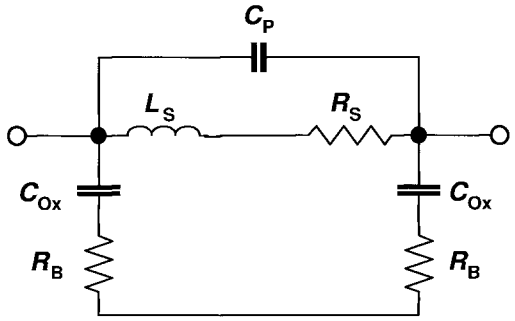


Fig. 6. Lumped-element model of the inductors.

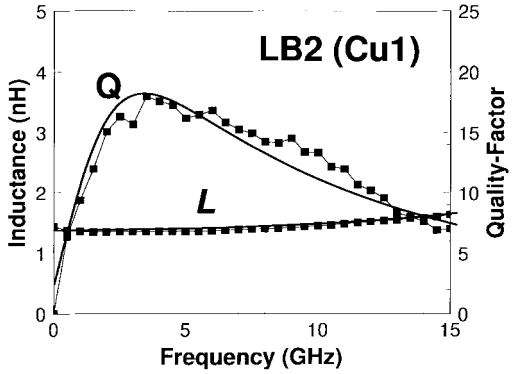


Fig. 7. Measured inductance and Q-factor as a function of frequency in comparison to the simulated characteristics derived from the lumped-element model in Fig. 6, with values from Table III.

TABLE III
LUMPED-ELEMENT PARAMETERS (FIG. 6) OF INDUCTORS $LB2$ BUILT BY USING THE PROCESSES Cu1–Cu3

Process	Rs (ohm)	Ls (nH)	Cp (pF)	Cox (pF)	Rb (ohm)
Cu1	0.75	1.25	0.02	0.25	550
Cu2	1.05	1.32	0.03	0.25	1800
Cu3	0.8	1.32	0.03	0.02	1400

in Table III, as well as those for $LB2$ fabricated by using the processes Cu2 and Cu3. From Table III, one can notice that the values for R_S and L_S are very similar to the measured data in Table IV. The values of $C_{\rm Ox}$ for Cu1 and Cu2 were identical and exceeded somewhat the value one would calculate for a plate capacitor that extends over the entire inductor area [7]. The difference in substrate resistivity appeared in the values of R_B of the two devices. In contrast to the other model elements, R_B has to be considered strictly a fitting parameter instead of a quasi-physical parameter. The comparison of Cu3 to Cu2 shows that with the sapphire substrate, not only R_B is high, but also $C_{\rm Ox}$ is significantly reduced.

From the lumped-element network in Fig. 6 and the parameters in Table III, it is obvious that at low frequencies Q is approximately $\omega L_S/R_S$, while at high frequencies a significant fraction of the signal can pass through the substrate (represented by $C_{\rm Ox}$ and R_B), reducing Q. Therefore, the

TABLE IV
CHARACTERISTIC PARAMETERS OF LB- AND LA-TYPE INDUCTORS FABRICATED BY USING THE CU–DAMASCENE (Cu1–Cu3) OR THE AL (Al1, Al2) PROCESSES

	LB2			LB5			LB8		
	Rdc (ohm)	L0 (nH)	Qmax (f/GHz)	Rdc (ohm)	L0 (nH)	Qmax (f/GHz)	Rdc (ohm)	L0 (nH)	Qmax (f/GHz)
Al1	1.7	1.35	10.6 (3.7)	2.35	2.15	8.8 (3.8)	4.46	4.90	7.2 (2.3)
Al2	0.65	1.45	24 (2.3)	1.04	2.20	16 (2.0)	2.05	5.10	11.5 (1.8)
Cu1	0.75	1.35	18 (3.7)	0.93	2.13	14 (3.5)	1.76	4.90	11.0 (2.1)
Cu2	1.05	1.40	30 (5.2)	1.15	2.20	25 (4.1)	2.38	4.95	16 (4.3)
Cu3	0.67	1.39	40 (5.8)	1.00	2.15	33 (5.6)	1.90	4.95	17 (4.1)

	LA2			LA4		
	Rdc (ohm)	L0 (nH)	Qmax (f/GHz)	Rdc (ohm)	L0 (nH)	Qmax (f/GHz)
Al1	32.1	86	3.0 (0.3)	4.80	16.9	5.4 (1.0)
Al2	---	---	---	---	---	---
Cu1	13.9	80	8.0 (0.3)	2.80	16.3	10.0 (0.5)
Cu2	16.8	80	9.4 (0.6)	3.40	16.3	14 (1.4)
Cu3	14.9	80	13 (0.6)	3.00	16.2	17.5 (1.9)

maximum value of Q, and the frequency at which it occurs, must be set by carefully tailoring R_S, $C_{\rm Ox}$, and R_B. The value of R_B was large enough in all cases to suppress self-resonance via $C_{\rm Ox}$ (impedance change from inductive to capacitive). Instead, self-resonance occurred via C_P, which was small in all cases, so that the frequency at which self-resonance was observed was much beyond the frequency at which the maximum Q ($Q_{\rm max}$) develops. That means that for all inductors fabricated, the inductance varied very little within the frequency range of interest (Figs. 4 and 5). Although the Cu thickness was designed to be the same for all three Cu processes, the wafer Cu2 required some rework during processing resulting in a somewhat thinner $M3$ layer, as mentioned in Section II (Table I). This was obvious from the difference in the dc resistances (Table IV) and in the slopes of Q *versus* frequency at low frequency (Figs. 4 and 5). The different decays of Q at high frequency for Cu1–Cu3 was a result of the different substrate types used. It was obvious that for both the HRS (Cu2) and the sapphire (Cu3) substrates this resulted in a significantly higher $Q_{\rm max}$. It is worth noting that for the sapphire substrate, the decay of Q at high frequencies was more pronounced and occurred at lower frequency than one would expect from a dielectric material that has a loss tangent $<$0.001 [13]. However, the loss tangent extracted from the electrical measurements of the sapphire substrate inductors was of the order of 0.05. We assumed that this was caused by Cu residuals in the field regions due to insufficient polishing (see Section II), which could be visually identified on the wafer. Nevertheless, the highest $Q_{\rm max}$ values were measured for the Cu3 process.

The benefit of the Cu metallization and the low-loss substrates can be brought into perspective through a comparison to conventional inductor implementations. The inductor $LB2$ with three levels of Cu interconnects, but a standard silicon substrate (Cu1), had a $Q_{\rm max}$ that came close to the one achieved with five Al levels (Al2), as shown in Table IV [6], [7]. The comparison of Cu1 and Al2 indicated that a single Cu–damascene layer can nearly substitute for three shunted Al

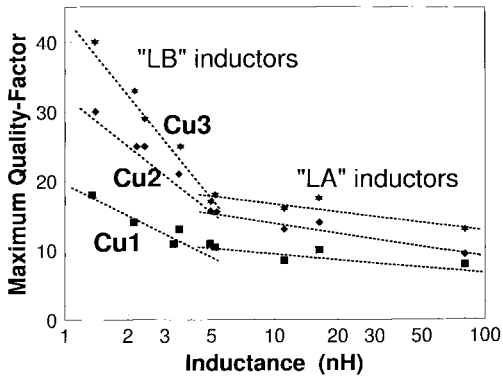


Fig. 8. Maximum Q factors drawn versus the inductances of different spiral inductors. LB-type inductors have an area of 226 × 226 μm^2; the area of the LA-type devices is 500 × 500 μm^2. (The figure includes the results from inductors which are not listed in Tables II and IV.)

layers. The $Q_{\max}$ of Cu1 was about 1.7 times greater than in a comparable three-level Al structure Al1 [15]. With use of the HRS substrate, the $Q_{\max}$ was raised to 30, and for the sapphire substrate, raised to even 40. This represents an improvement of about 1.7 times over the $Q_{\max}$ of 24 in [6], [7] for the five-level metal structure and a 3.8 times increase over the three-level Al process Al1. A similar degree of improvement with the low-loss substrates Cu2 and Cu3 was observed for the other two inductors of the same area size, $LB5$ and $LB8$, which had been discussed in [6], [7] as well (see Table IV). Greater increases were achieved for the large-area structures ($LA2$ and $LA4$), as is obvious from Table IV, because with the larger number of turns, the effect of the coil resistance was more pronounced. Even though the $Q_{\max}$ becomes typically smaller at large inductance values [7], a $Q_{\max}$ of 13 was measured for the 80-nH inductor $LA2$ fabricated by using the process Cu3.

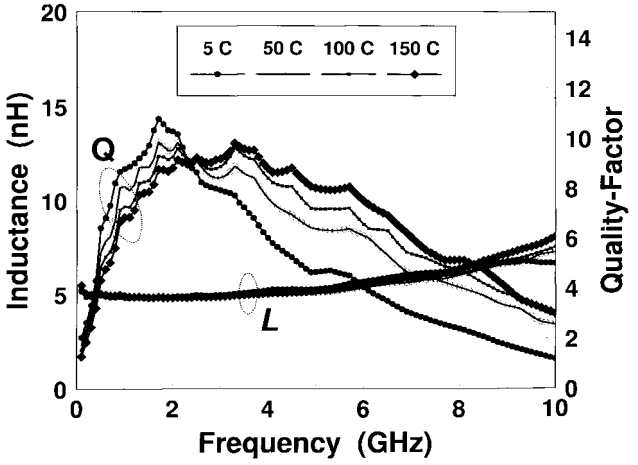
Fig. 8 shows the $Q_{\max}$ values of all fabricated inductors drawn *versus* the inductances. It is first obvious that the reduction in substrate losses translates into higher $Q_{\max}$ values over the entire range of inductances. For each inductor area-size (LB-type or LA-type) there was a clear trend that smaller inductances combine with higher $Q_{\max}$ values and vice-versa [7]. The slope of $Q_{\max}$ versus L, however, was larger for the small-area (LB-type) structures compared to the LA-type, so that beyond 5-nH inductance the LA-inductor structures provided the higher $Q_{\max}$. This indicated that besides the process technology improvement discussed in the bulk of this paper, the lateral inductor geometry must also be carefully optimized to achieve the highest possible $Q_{\max}$.

The inductances and $Q's$ of inductor types $LB8$ (Table II) were measured at various temperatures in order to receive further insight into the relevance of the different parameters which determine the electrical inductor characteristics. Since the changes of the geometrical dimensions of the inductor spiral with temperature were expected to be comparably small, the resistivities of the metal and of the substrate were likely dominating the temperature dependence of the inductors [16], [17]. The temperature coefficient of the metal is typically positive. The same can be expected for the substrate resistance below the temperature at which the intrinsic carrier concentration becomes comparable to the background doping of the substrate silicon. Below that point, the carrier mobility is approximately proportional to $T^{-2.3}$ [16], so that R_B (Fig. 6) will increase by about a factor of three within the temperature range from 5 to 150 °C used in our measurements. This will lead to an increasing Q at high frequency with temperature (*delayed* fall-off of Q in Figs. 4 and 5). For the HRS substrate (Cu2) with a background doping concentration in the range of $\sim 10^{13}$ cm^{-3}, the intrinsic carrier concentration will overcome the background doping level at temperatures from 100 to 150 °C [16]. In that temperature range, R_B will decrease because the carrier concentration starts to increase rapidly with temperature, which starts to dominate over the carrier mobility reduction. As a result, Q will decay more rapidly at high temperature. For the conventional substrate (Cu1) this transition point is beyond 200 °C, so that one would expect R_B to monotonically increase within the range of the measurements.

These anticipated temperature characteristics are confirmed by our measurements of the inductor $LB8$ that was fabricated over each type of substrate (Cu1–Cu3). For an improved accuracy, we remeasured the contact-pad dummy device (Section II) at each temperature. The measured inductances and Q factors at each temperature drawn *versus* frequency are shown in Fig. 9(a)–(c). For the inductor built over the 10-Ωcm silicon substrate (Cu1), the qualitative change in the electrical characteristics was similar to the observations in [17]. The coil resistance increased with temperature, which led to a smaller increase of Q with frequency at low frequencies, and the increase in R_B due to the carrier mobility reduction lowering the slope of the fall-off of Q at high frequencies [see Fig. 9(a)]. This result was also confirmed by measuring the same inductor fabricated with the process Al1. For the HRS (Cu2), the situation was similar only up to 100 °C. At 100 and 150 °C, the decay of Q at high frequencies became more pronounced with increasing temperature so that $Q_{\max}$ became considerably smaller at high temperature [see Fig. 9(b)]. This seemed to indicate that the intrinsic carrier concentration is of the same order of magnitude or higher than the background doping of the HRS material at those temperatures. For the sapphire substrate (Cu3), clear differences were only observed at low frequencies at which the temperature dependence of the Cu dominates the device characteristics. The change in the fall-off of Q with temperature at the higher frequencies was negligibly small, which confirms the impact of R_B in the other two cases [see Fig. 9(c)]. The change in the inductance value with temperature was very small at low frequencies for all types of substrates.

IV. Transmission Lines

Various types of transmission lines, which used either two levels of metal [microstrip [Fig. 2(a)] and inverted microstrip [Fig. 2(b)]] or only the $M3$ level [coplanar line [Fig. 2(c)]], were fabricated. Two-port S-parameters were measured *without de-embedding the contact pad parasitics* (Section II). All structures had a length of 17 600 μm and were fabricated on either the 10-Ωcm silicon (Cu1) or the HRS (Cu2) substrates.



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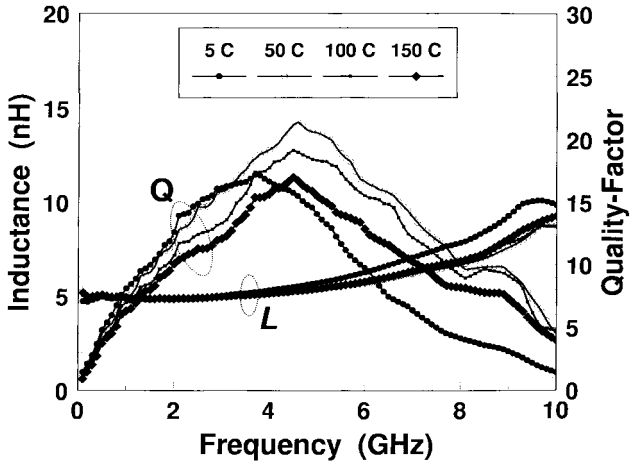

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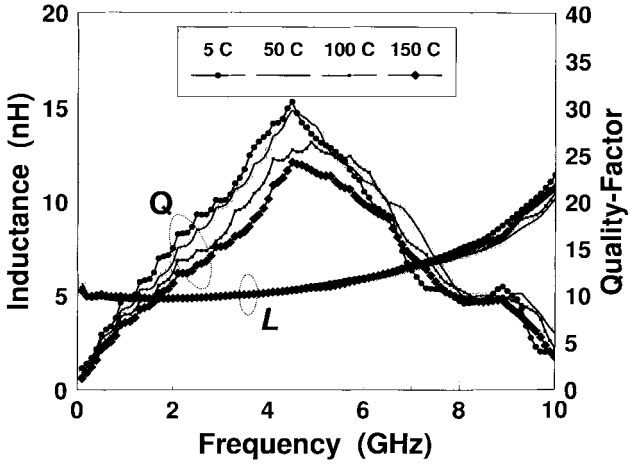
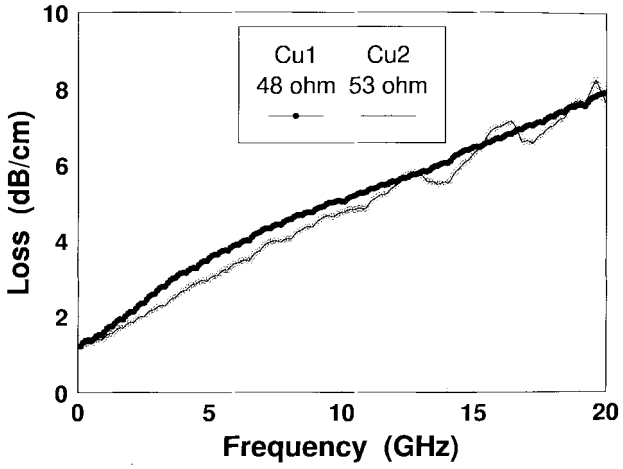
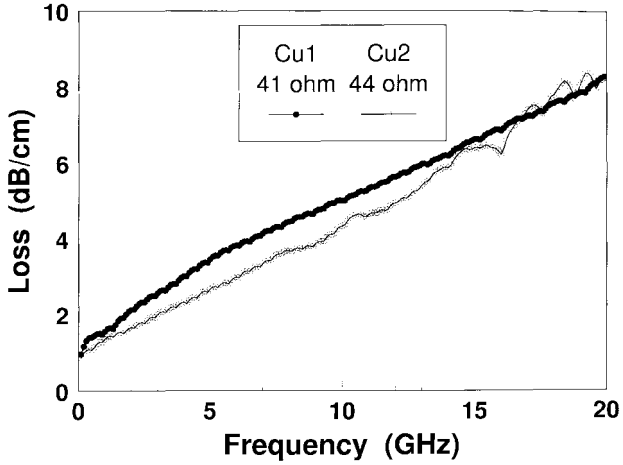


(c)

Fig. 9. Inductances and Q factors of device $LB8$ drawn *versus* frequency at various temperatures. The 10-Ωcm silicon (a) Cu1, (b) HRS Cu2, and (c) sapphire Cu3 substrates are compared.



(a)



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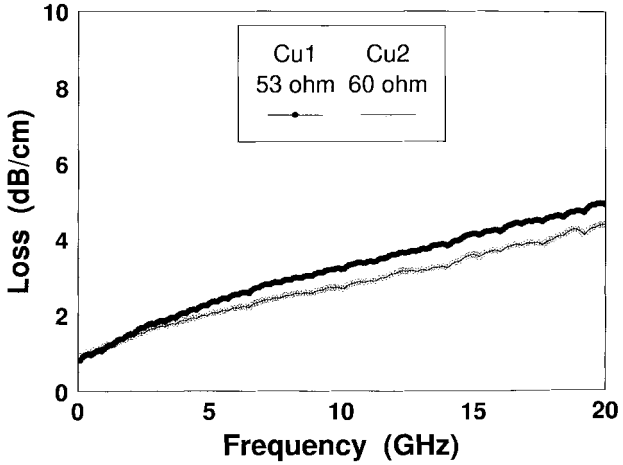

(c)

Fig. 10. Losses versus frequency of (a) microstrip lines (Fig. 2(a), $W = 6$ μm, $W_G = 20$ μm), of (b) inverted microstrip lines (Fig. 2(b), $W = 4$ μm, $W_G = 20$ μm), and of (c) coplanar transmission lines ($W = 8$ μm, $S = 5$ μm, $W_G = 40$ μm). For each, the 10-Ωcm silicon (Cu1) and the HRS (Cu2) substrates are compared.

A difference from conventional implementations was (besides the considerable losses in the substrates) that the ground planes of microstrip and inverted microstrip had limited widths. This appeared relevant for an integration of an RF transceiver in which the interconnects are shared between the transmission lines and the internal metallization of the circuits. The losses per unit length *versus* frequency of transmission lines built either over 10-Ωcm silicon (Cu1) or over HRS (Cu2) are shown in Fig. 10(a)–(c) (via linear extrapolation from mea-

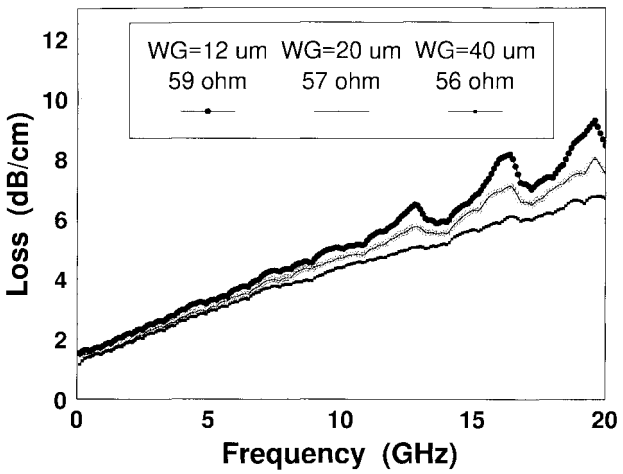

Fig. 11. Losses of microstrip transmission lines with identical width ($W = 4$ μm) and different widths of the ground plane (W_G) as a function of frequency (HRS substrate). (The evident signal oscillations are a result of the change in line impedance at the contact pads.)

sured S_{21} magnitudes). The comparison of the microstrip line [Fig. 10(a)] to the inverted microstrip [Fig. 10(b)] line shows that the position of the ground plane in between the substrate and the conductor has some advantage in shielding against the substrate. However, for that reason the effect of the substrate type on the loss was rather small. The apparent difference was most distinct at low frequencies (<5 GHz) where the slope of the losses *versus* frequency was slightly larger for the Cu1 substrate compared to Cu2. This resulted from the fact that the conduction of majority carriers is invariant with frequency while the dielectric polarization losses increase with frequency. Therefore, ohmic losses (eddy–currents) dominated at low frequencies and losses due to dielectric polarization dominated at high frequency [11]. For the coplanar transmission line in Fig. 10(c), the relative difference between the Cu1 and Cu2 substrates was similar to that of the inverted microstrip. The absolute loss was lower for the coplanar line because the conductor was wider (8 versus 4 μm), but this difference was largely compensated by the thicker $M2$ layer [4 versus 2.4 μm, (Section II)]. Fig. 11 shows the losses of three microstrips with identical widths ($W = 4$ μm) but differently wide ground planes (W_G), all built over HRS substrates. At low frequency, the losses were dominated by ohmic power dissipation in the conductor and by Eddy currents in the ground planes, and differences between the three structures were small. At high frequency where the polarization losses in the silicon dominate, the loss was smaller as the ground plane became wider. This showed that the ground plane was effective in shielding against the silicon substrate.

The transmission-line losses established here were very comparable to those published by Reyes *et al*. [11] if one considers their Au coplanar transmission lines over >3000-Ωcm silicon substrates with dielectric isolation in between. However, they showed that by omitting the dielectric isolation, one can form a Schottky (metal–semiconductor) junction and thus deplete the silicon surface of mobile carriers. This resulted in a reduction of the losses by a factor of ten. This concept, even though effective, does not seem compatible with planar silicon-fabrication processes. Another loss reduction by a factor of about two was found for Au metallization over quartz substrates, but this type of substrate is not used in silicon technology as well. If one restricts the discussion to strictly silicon-compatible processing, our results were in line with the least lossy transmission-line implementations demonstrated to date. Given the low-loss per line length, the loss can be kept down to a few decibels even for transmission lines of maximum length on typical-size silicon chips. The microstrip line seems preferable over coplanar transmission lines in integrated RF systems for two reasons: the overall width of a coplanar line is considerably larger than that of a microstrip because it uses only a single metal layer, and multilevel metallization is readily available in silicon technology so that the main reason for choosing a coplanar line (i.e., the fact that only a single metal layer is required) vanishes.

V. Conclusion

Spiral inductors and different types of transmission lines have been fabricated by using Cu–damascene interconnects over HRS or sapphire substrates, as well as over conventional silicon substrates for control purposes. The measured inductor-Q values and transmission-line losses seem adequate for fabricating RF transceiver systems on silicon substrates. Combined with the HRS substrate, the Cu interconnect technology is fully compatible with VLSI silicon processing and produces an inductor-Q that is about three times that achievable by using a commercially available silicon-fabrication processes with the same number of metal levels.

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